

FIG. 1

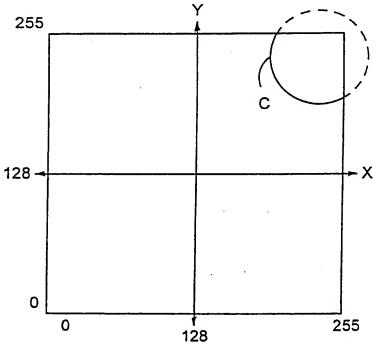
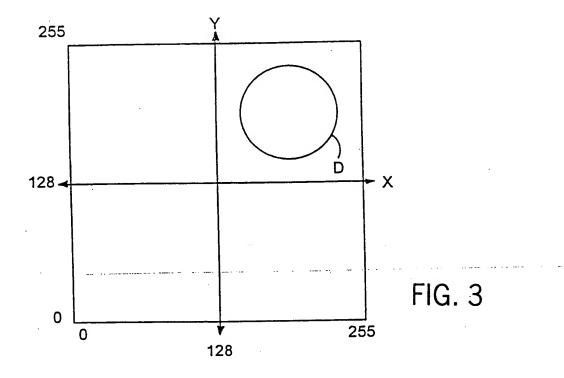


FIG. 2



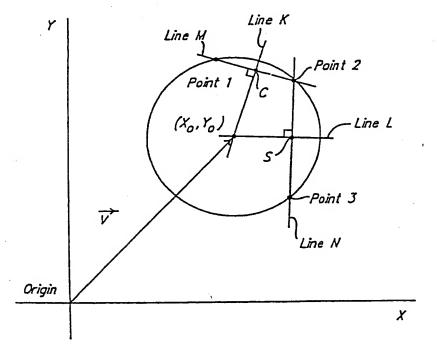
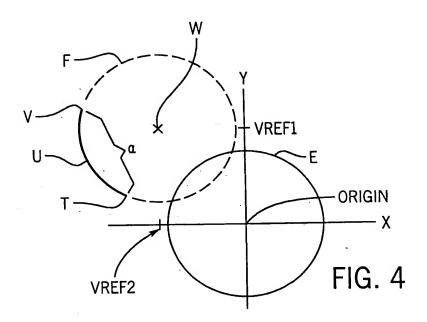
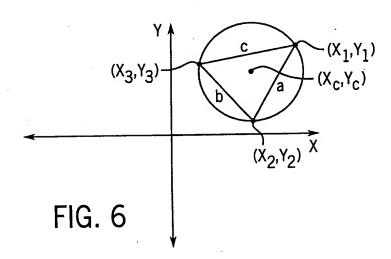
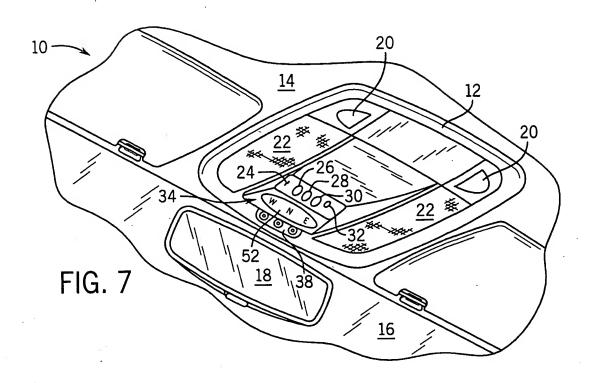
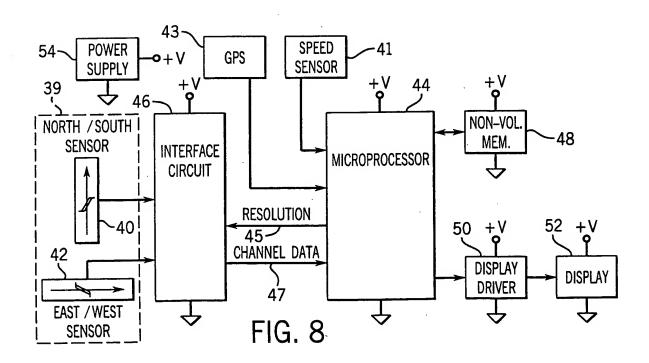


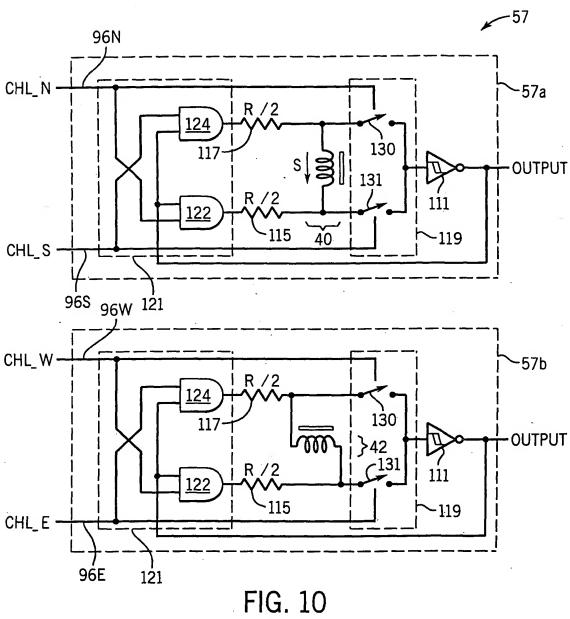
FIG. 5

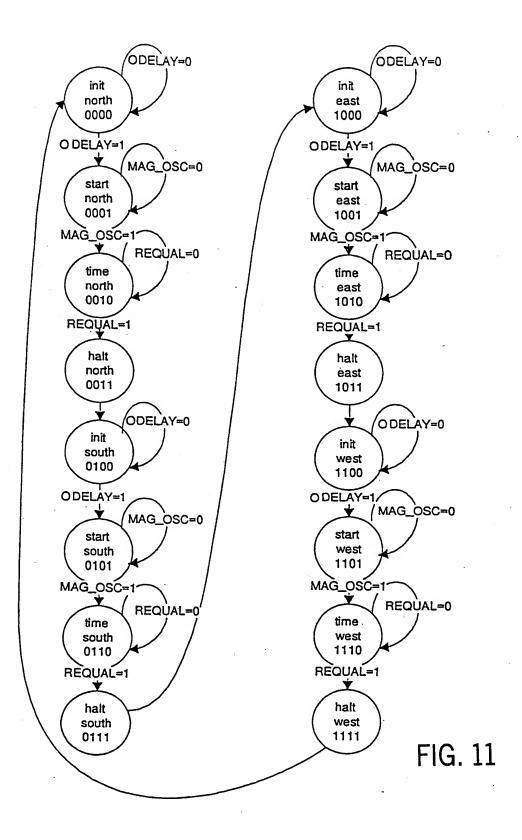












STATE DESCRIPTION ROLEARU DELAY(I) REMABLE_E(I) (CLEARO) U /D(IO) ENABLE(I) LATCH_N(IO) LATCH_E(IO) (CHL_N(IO) CHL_S(IO) CHL_E(IO) (CHL_N(IO) CHL_S(IO) CHL_E(IO) (CHL_N(IO) CHL_S(IO) CHL_R(IO) CHL_N(IO) CHL_S(IO) CHL_R(IO) CHL_N(IO) CHL			1	т-	T	T-		T	Γ.	_	1					T	Γ-	$\Box$
DESCRIPTION   RCLEAR(I)   DELAY(I)   RENABLE_E(I)   CLEAR(I)   DILAY(I)   RENABLE_E(I)   CLEAR(I)   DILAY(I)   RENABLE_E(I)   CLEAR(I)   DILAY(I)   DILAY(I)   RENABLE_E(I)   CLEAR(I)   DILAY(I)		CHL_W(0	0	0	0	0	0	0	0	0	0	0	0	0	7	1		0
DESCRIPTION   RCLEAR(1)   DELAY(1)   RENABLE_E(1)   CLEAR(0)   U / D(0)   ENABLE(1)   LATCH_N(0)   LATCH_N(		CHL_E(0)	0	0	0	0	0	0	0	0	1		П	0	0	0	0	0
DESCRIPTION   RCLEAR(1)   DELAY(1)   RENABLE_E(1)   CLEAR(0)   U / D(0)   ENABLE(1)   LATCH_N(0)   LATCH_N(		CHL_S(0)	0	0	0	0	-		1	0	0	0	0	0	0	0	0	0
DESCRIPTION   RCLEAR(1)   DELAY(1)   RENABLE_E(1)   CLEAR(10)   U / D(10)   ENABLE(1)   LATCH_E(10)   LATCH_E(10	*	CHL_N(0)	-	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
DESCRIPTION   RCLEAR(I)   DELAY(I)   RENABLE_E(I)   CLEAR(O)   U / D(O)   ENABLE(I)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
DESCRIPTION RCLEAR(1) [ INITIALIZE NORTH 1 START NORTH 0 START TIMING NORTH 1 INITIALIZE SOUTH 1 START SOUTH 0 START TIMING SOUTH 0 START TIMING SOUTH 1 INITIALIZE EAST 1 START TIMING EAST 0 START TIMING EAST 0 START TIMING WEST 0	COMPASS STATE MACHINE STATE OUTPUT MATRIX	LATCH_N(0)	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0
DESCRIPTION RCLEAR(1) [ INITIALIZE NORTH 1 START NORTH 0 START TIMING NORTH 1 INITIALIZE SOUTH 1 START SOUTH 0 START TIMING SOUTH 0 START TIMING SOUTH 1 INITIALIZE EAST 1 START TIMING EAST 0 START TIMING EAST 0 START TIMING WEST 0		ENABLE(1)	-1	-	·O				0			-	0			1	0	-1
DESCRIPTION RCLEAR(1) [ INITIALIZE NORTH 1 START NORTH 0 START TIMING NORTH 1 INITIALIZE SOUTH 1 START SOUTH 0 START TIMING SOUTH 0 START TIMING SOUTH 1 INITIALIZE EAST 1 START TIMING EAST 0 START TIMING EAST 0 START TIMING WEST 0		(0)Q/ N	0	0	0					0	0	0	0	1				0
DESCRIPTION RCLEAR(1) [ INITIALIZE NORTH 1 START NORTH 0 START TIMING NORTH 1 INITIALIZE SOUTH 1 START SOUTH 0 START TIMING SOUTH 0 START TIMING SOUTH 1 INITIALIZE EAST 1 START TIMING EAST 0 START TIMING EAST 0 START TIMING WEST 0		CLEAR(0)	0	0							0	0	-		-		-	
DESCRIPTION RCLEAR(1) [ INITIALIZE NORTH 1 START NORTH 0 START TIMING NORTH 1 INITIALIZE SOUTH 1 START SOUTH 0 START TIMING SOUTH 0 START TIMING SOUTH 1 INITIALIZE EAST 1 START TIMING EAST 0 START TIMING EAST 0 START TIMING WEST 0		RENABLE_E(1)	1			,	,1				0	0	0	0	0	0	0	0
DESCRIPTION INITIALIZE NORTH START TIMING NORTH HALT TIMER INITIALIZE SOUTH START TIMING SOUTH ALT TIMER INITIALIZE EAST START TIMING EAST START TIMING EAST START TIMING EAST START TIMING WEST		DELAY(1)	0	1	1	1	0	1	1	1	0	1	1	1	0	-1	1	1
		RCLEAR(1)	1	0	0	1	1	0	0	1		0	0	Ţ	1	0	0	
		DESCRIPTION	INITIALIZE NORTH	START NORTH	START TIMING NORTH	HALT TIMER	INITIALIZE SOUTH	START SOUTH	START TIMING SOUTH	HALT TIMER	INITIALIZE EAST	START EAST	START TIMING EAST	HALT TIMER	INITIALIZE WEST	START WEST	START TIMING WEST	HALT TIMER
		STATE	0000	0001		0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101		
0178470978601171843			0		7	က	4	ည	9	7	∞	6	10	11	12	13	14	15

FIG. 12

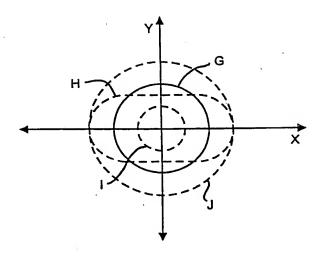
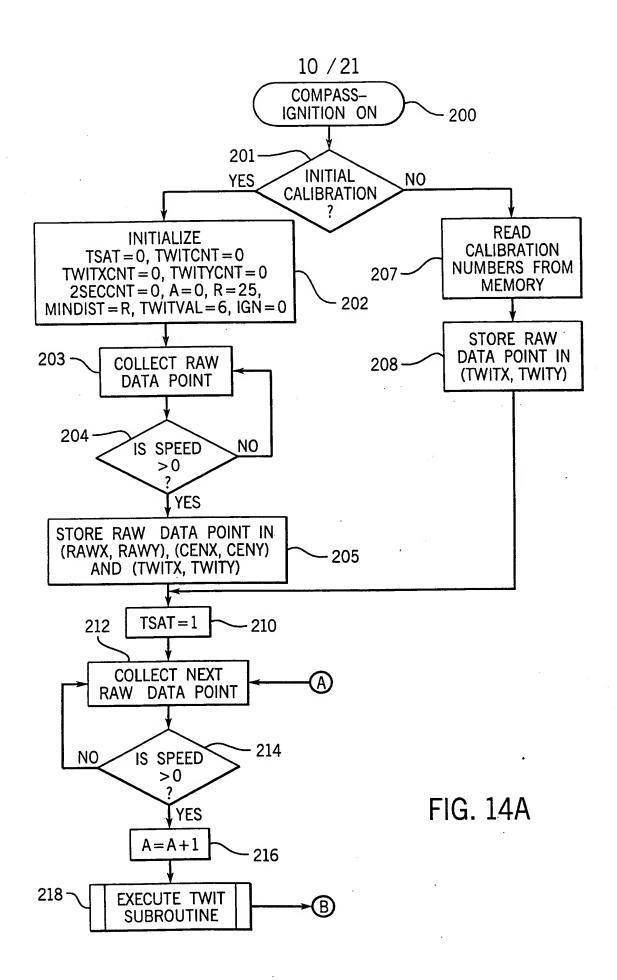
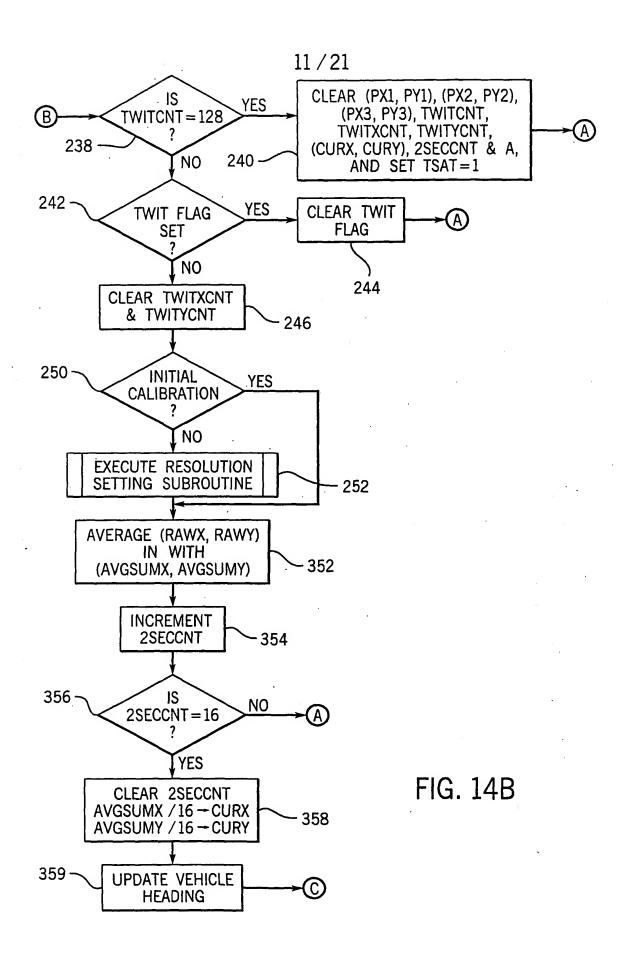
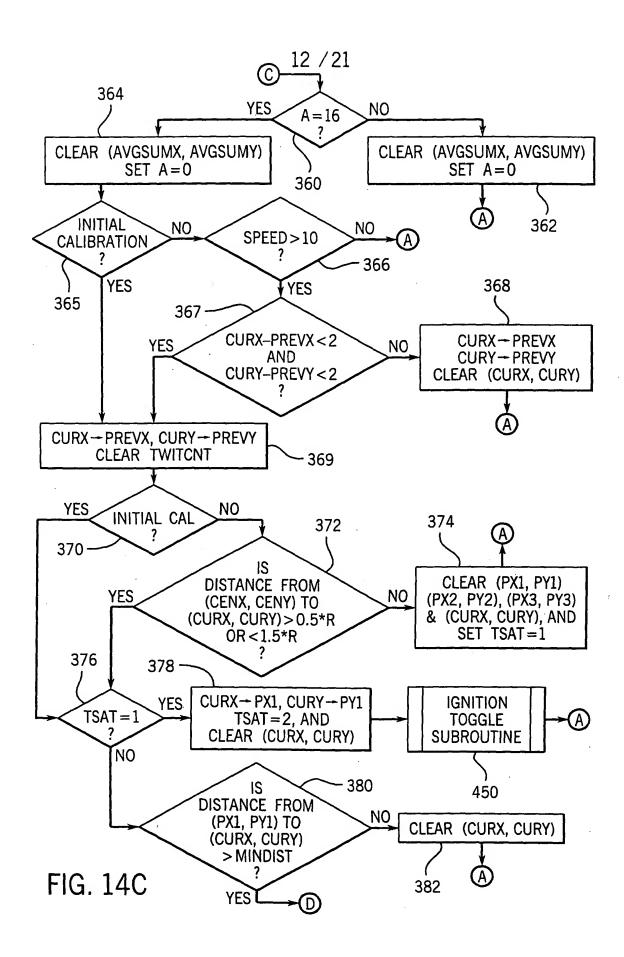
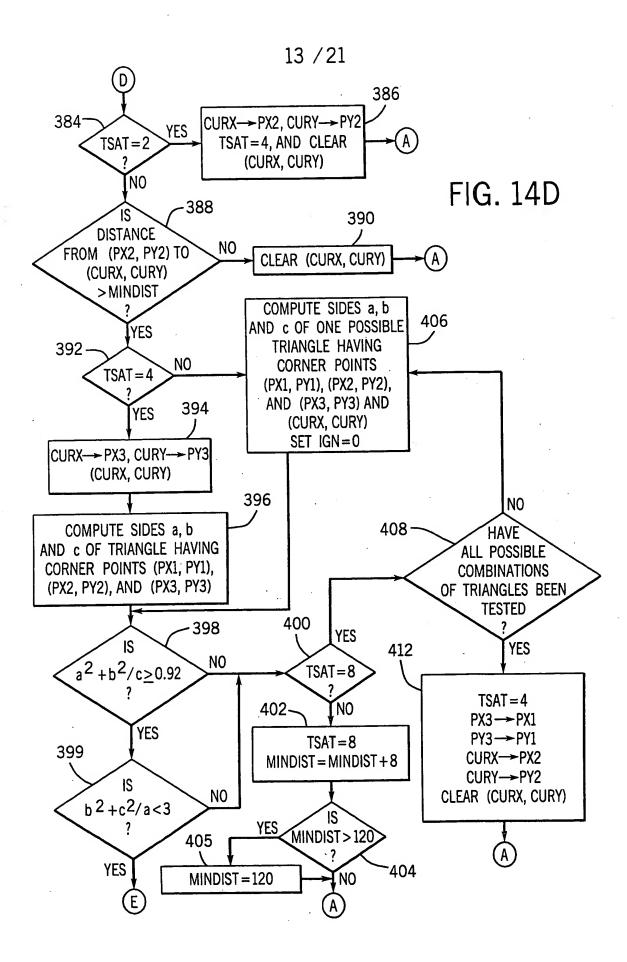


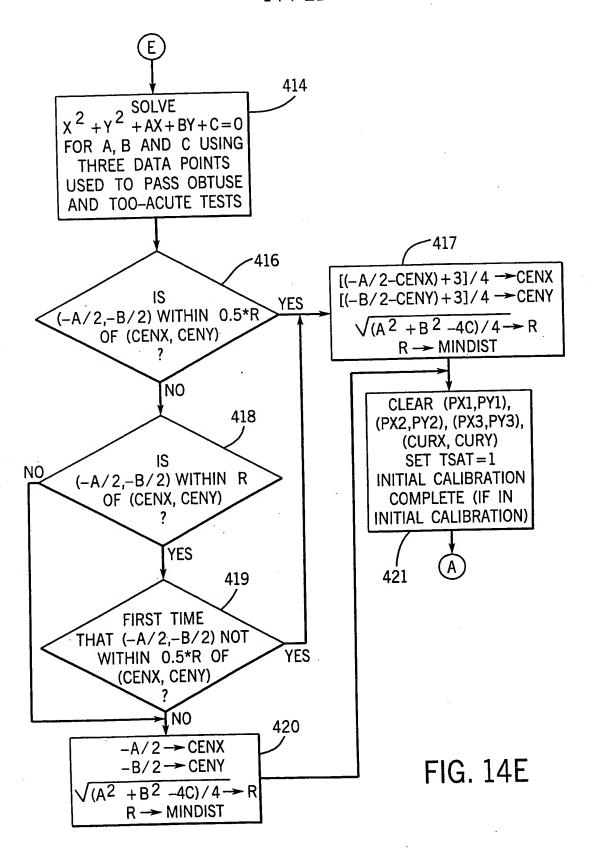
FIG. 13











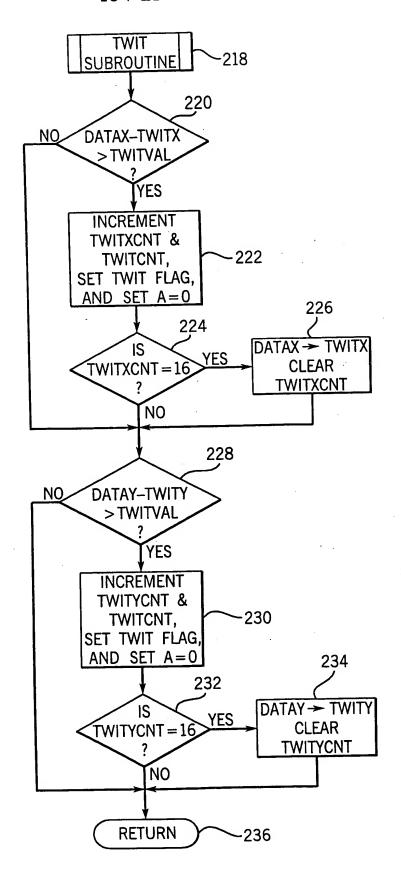


FIG. 15

